

CLAIMS:

1. A frequency divider circuit comprising:
an even number of amplifier stages connected in
5 series with the output of the last amplifier stage
connected to the input of the first amplifier stage; and
modulating means, responsive to an input signal to
be frequency divided, for modulating the propagation
10 delay through each of said amplifier stages, about the
period of the input signal to be divided, such that when
the propagation delay through the odd amplifier stage(s)
increases, the propagation delay through the even
amplifier stage(s) decreases.
- 15 2. A frequency divider circuit according to claim 1,
wherein there are two amplifier stages connected in
series.
3. A frequency divider circuit comprising a plurality
20 of frequency divider circuits according to claim 1 or 2
connected in series.
4. A frequency divider circuit according to claim 1,
2 or 3, wherein each amplifier is a differential
25 amplifier.
5. A frequency divider circuit according to any
preceding claim, wherein each amplifier stage comprises
an amplifier with hysteresis.
- 30 6. A frequency divider circuit according to any
preceding claim, wherein said modulating means varies the
strength of connection between adjacent amplifier stages.
- 35 7. A frequency divider circuit according to claim 5,

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8. A frequency divider circuit according to any
5 preceding claim, wherein said frequency divider circuit
is a FET type semiconductor circuit.

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two inverters connected in a memory arrangement with

input means connected to said memory arrangement,
for writing new data applied to said data input into said
5 memory arrangement, in dependence upon a clock signal
applied to said clock input;

10 said latch comprises varying means for varying the
time taken for new data to be written into said memory
arrangement.

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modulating the propagation delay through each of said amplifier stages, about the period of the input signal to be divided, such that when the propagation delay through odd-numbered amplifier stage(s) increases, the propagation delay through even-numbered amplifier stage(s) decreases.

22. A method according to claim 20 or 21, wherein each amplifier stage used comprises an amplifier with hysteresis.

20 24. A method according to claim 22, wherein said
modulating step varies the hysteresis of each of said
amplifier stages.

26. A method according to claim 25, wherein said amplifier stages comprise a CMOS integrated circuit.

35 28. A method according to any of claims 20-27, wherein

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so uses logic circuits
ios other than simple po
ceiver comprising a fr
ng to any of claims 1 to
uency division according
receiver comprising a
y of claims 13 to 19.

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